

FORM PTO-1390  
(REV 10-2000)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER

B-4277PCT 619004-9

TRANSMITTAL LETTER TO THE UNITED STATES  
DESIGNATED/ELECTED OFFICE (DO/EO/US)  
CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)  
**09/913452**  
not yet assigned

INTERNATIONAL APPLICATION NO.  
PCT/GB00/00528

INTERNATIONAL FILING DATE  
15 February 2000

PRIORITY DATE CLAIMED  
15 February 1999

TITLE OF INVENTION

TRUSTED COMPUTING PLATFORM

APPLICANT(S) FOR DO/EO/US (1) Graeme John PROUDLER (2) Dipankar GUPTA (3) Liqun CHEN  
(4) Siani Lynne PEARSON (5) Boris BALACHEFF (6) Bruno Edgard VAN WILDER (7) David CHAN

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
  - a. ☒ is attached hereto (required only if not communicated by the International Bureau).
  - b. ☐ has been communicated by the International Bureau.
  - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(3)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
  - a. ☐ are attached hereto (required only if not communicated by the International Bureau).
  - b. ☐ have been communicated by the International Bureau.
  - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
  - d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 16 below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A **FIRST** preliminary amendment.  
☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:

copy of Published Title Page of PCT International Application  
copy of PCT Request  
copy of PCT Demand  
copy of International Preliminary Examination Report  
Claim to Priority  
copy of International Search Report (see Information Disclosure Statement)

U.S. APPLICATION NO. (if known, see 37 CFR 1.51)  
not yet assigned

09/913452

INTERNATIONAL APPLICATION NO.  
PCT/GB00/00528ATTORNEY'S DOCKET NUMBER  
B-4277PCT 619004-917. ☒ The following fees are submitted:**BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :**

Neither international preliminary examination fee (37 CFR 1.482)  
nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO  
and International Search Report not prepared by the EPO or JPO ..... \$1000.00

International preliminary examination fee (37 CFR 1.482) not paid to  
USPTO but International Search Report prepared by the EPO or JPO. .... \$860.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but  
international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... \$710.00

International preliminary examination fee paid to USPTO (37 CFR 1.482)  
but all claims did not satisfy provisions of PCT Article 33(1)-(4) ..... \$690.00

International preliminary examination fee paid to USPTO (37 CFR 1.482)  
and all claims satisfied provisions of PCT Article 33(1)-(4) ..... \$100.00

**ENTER APPROPRIATE BASIC FEE AMOUNT =****CALCULATIONS PTO USE ONLY**

\$ 860.00

Surcharge of \$130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30  
months from the earliest claimed priority date (37 CFR 1.492(e)).

\$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE
Total claims	38 - 20 =	18	X \$18.00
Independent claims	5 - 3 =	2	X \$80.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable) 0*			+ \$270.00

\$ 324.00

\$ 160.00

\$ 0

**TOTAL OF ABOVE CALCULATIONS =**

\$ 1,344.00

☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above  
are reduced by 1/2.

\$

**SUBTOTAL =**

\$ 1,344.00

Processing fee of \$130.00 for furnishing the English translation later than ☐ 20 ☐ 30  
months from the earliest claimed priority date (37 CFR 1.492(f)).

\$

+

**TOTAL NATIONAL FEE =**

\$ 1,344.00

Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be  
accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property

\$

+

**TOTAL FEES ENCLOSED =**

\$ 1,344.00

\*Preliminary Amendment  
deleting multiple dependencies  
enclosed herewith.

Amount to be

refunded:

\$

charged:

\$

a. ☒ A check in the amount of \$ 1,344.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. \_\_\_\_\_ in the amount of \$ \_\_\_\_\_ to cover the above fees.  
A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any  
overpayment to Deposit Account No. 12-0415. A duplicate copy of this sheet is enclosed.

**NOTE:** Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

AUGUST 14, 2001

DATE

LADAS & PARRY  
5670 Wilshire Blvd., #2100  
Los Angeles, California 90036-5679  
Telephone No.: (323) 934-2300  
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SIGNATURE

Richard P. Berg

NAME

28,145

REGISTRATION NUMBER

09/913452

EL652176579USIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Graeme John	)	Re: Preliminary Amendment
PROUDLER, et al.	)	
	)	
U.S. Appln. No.: not yet	)	Group: not yet assigned
assigned	)	
	)	
U.S. Filing Date: concurrently	)	Examiner: not yet assigned
herewith	)	
	)	
International Application No:	)	
PCT/GB00/00528	)	
International Filing Date:	)	
15 February 2000	)	Our Ref.: B-4277PCT 619004-9
	)	
For: "TRUSTED COMPUTING	)	
PLATFORM"	)	Date: August 14, 2001

Commissioner of Patents and Trademarks  
 Box PCT  
 Washington, D.C. 20231

Attn: United States Designated/Elected Office (DO/EO/US)

Sir:

Prior to examination of the above-identified application, it is respectfully requested that the following amendments be made to the Claims:

IN THE CLAIMS

1. (Amended) Computing apparatus comprising, mounted on an assembly, main processing means, main memory means and a trusted device, each being connected for communication with one or more other components on the assembly,

the trusted device being arranged to acquire a true value of an integrity metric of the computing apparatus.

4. (Amended) Computing apparatus according to claim 3, wherein the computing apparatus is arranged to cause the instructions to be the first instructions executed after release from reset.

Re: Preliminary Amendment  
August 14, 2001  
Page 2

5. (Amended) Computing apparatus according to claim 3, wherein the trusted device is arranged to transfer the instructions to the main processing means in response to memory read signals from the main processing means.

6. (Amended) Computing apparatus according to claim 1, wherein the trusted device comprises device memory means and is arranged to monitor a data bus means by which components mounted on the assembly are adapted to communicate and store in the device memory means a flag in the event the first memory read signals generated by the main processing means after the computing apparatus is released from reset are addressed to the trusted device.

7. (Amended) Computing apparatus according to claim 1, wherein the trusted device has stored in device memory means at least one of:

- a unique identity of the trusted device;
- an authenticated integrity metric generated by a trusted party; and
- a secret.

10. (Amended) Computing apparatus according to claim 8, wherein the trusted device has stored in device memory means an authenticated integrity metric generated by a trusted party and includes a encryption function, the trusted device being arranged to generate a response to a received challenge, the response comprising an acquired integrity metric and the authenticated integrity metric, both signed by the encryption function using the private asymmetric encryption key.

Please cancel claim 11 without prejudice.

12. (Amended) A method of operating a system comprising a trusted computing apparatus and a user, the trusted computing apparatus incorporating a trusted device being arranged to acquire the true value of an integrity metric of the trusted computing apparatus, the method comprising the steps of:

the trusted device acquiring the true value of the integrity metric of the trusted computing apparatus;

the user generating a challenge for the trusted computing apparatus to prove its integrity and submitting the challenge to the trusted computing apparatus;

the trusted computing apparatus receiving the challenge, and the trusted device generating a response including the integrity metric and returning the response to the user; and

the user receiving the response, extracting the integrity metric from the response and comparing the integrity metric with an authenticated metric for the trusted computing apparatus that had been generated by a trusted party.

16. (Amended) A method of establishing a communications channel in a system between trusted computing apparatus and remote computing apparatus, the method including the step of the remote computing apparatus verifying the integrity of the trusted computing apparatus using the method according to claim 12, and maintaining the communications channel for further transactions in the event the integrity of the trusted computing apparatus is successfully verified by the remote computing apparatus.

17. (Amended) A method of verifying that trusted computing apparatus is trustworthy for use by a user for processing a particular application, the method including the step of the user verifying the integrity of the trusted computing apparatus

using the method according to claim 12, and the user using the trusted computing apparatus to process the particular application in the event the integrity of the trusted computing apparatus is successfully verified by the remote computing apparatus.

Please cancel claims 18-21 without prejudice.

Please add the following new claims:

22. (New) Computing apparatus comprising an assembly; a main processor, a main memory and a trusted device, each being mounted on the assembly and connected for communication with other components mounted on the assembly, wherein the trusted device is adapted to acquire a value of an integrity metric that measures that the computing apparatus is operating as intended and determining the correctness of the acquired value of the integrity metric.

23. (New) Computing apparatus as claimed in claim 22, wherein the integrity metric is a digest of all or part of the basic input/output software for the computing apparatus.

24. (New) Computing apparatus as claimed in claim 22, wherein the integrity metric is a digest of all or part of the basic input/output software for components or apparatus attached to the computing apparatus.

25. (New) Computing apparatus as claimed in claim 22, wherein the trusted device is adapted to acquire a plurality of integrity metrics.

26. (New) Computing apparatus as claimed in claim 22, wherein

the trusted device is adapted to be tamper resistant.

27. (New) Computing apparatus as claimed in claim 22, wherein the trusted device comprises a device memory.

28. (New) Computing apparatus as claimed in claim 27, wherein the trusted device comprises a trusted device processor.

29. (New) Computing device as claimed in claim 28, wherein the trusted device processor is adapted to instruct the main processor to determine the integrity metric and return the integrity metric for storage in the device memory.

30. (New) Computing apparatus as claimed in claim 28, wherein the trusted device processor is adapted to obtain information necessary to calculate the integrity metric and to calculate the integrity metric for storage in the device memory.

31. (New) Computing apparatus as claimed in claim 28, wherein the trusted device has a secret stored in the device memory.

32. (New) Computing apparatus as claimed in claim 31, wherein the secret comprises a private asymmetric encryption key.

33. (New) Computing apparatus as claimed in claim 32, wherein the trusted device also has stored in the device memory in the device memory a respective public encryption key that has been signed by a trusted third party.

34. (New) Computing apparatus as claimed in claim 33, wherein the trusted device also has stored in the device memory an authenticated integrity metric generated by a trusted third party and wherein the trusted device is adapted to employ an

encryption function, the trusted device processor being arranged to generate a response to a received challenge, the response comprising an acquired integrity metric and the authenticated integrity metric, both signed by the encryption function using the private asymmetric encryption key.

35. (New) In a computing apparatus comprising an assembly, a plurality of functional components including a main memory and a main processor mounted on the assembly, each functional component being connected for communication with one or more other functional components on the assembly, a trusted device being one of said functional components and adapted to acquire a value of an integrity metric that measures that the computing apparatus is operating as intended and determining the correctness of the acquired value of the integrity metric.

36. (New) A trusted device for use as a functional component in a computing apparatus, the trusted device being adapted for mounting on an assembly of the computing apparatus and being adapted for communication with other functional components of the computing apparatus, the trusted device being adapted to acquire a value of an integrity metric that measures that the computing apparatus is operating as intended and determining the correctness of the acquired value of the integrity metric.

37. (New) Computing apparatus as claimed in claim 36, wherein the trusted device is adapted to be tamper resistant.

38. (New) Computing apparatus as claimed in claim 36, wherein the trusted device comprises a device memory.

39. (New) Computing apparatus as claimed in claim 38, wherein the trusted device comprises a trusted device processor.

40. (New) Computing apparatus as claimed in claim 39, wherein the trusted device has a secret stored in the device memory.

41. (New) Computing apparatus as claimed in claim 40, wherein the secret comprises a private asymmetric encryption key.

42. (New) Computing apparatus as claimed in claim 41, wherein the trusted device also has stored in the device memory in the device memory a respective public encryption key that has been signed by a trusted third party.

43. (New) Computing apparatus as claimed in claim 42, wherein the trusted device also has stored in the device memory an authenticated integrity metric generated by a trusted third party and wherein the trusted device is adapted to employ an encryption function, the trusted device processor being arranged to generate a response to a received challenge, the response comprising an acquired integrity metric and the authenticated integrity metric, both signed by the encryption function using the private asymmetric encryption key.

#### REMARKS

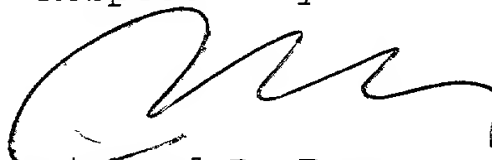
This Preliminary Amendment clarifies some of the terms in the claims. Such amendments to claims 1 and 2 do not affect the scope of those claims. New claims 22-43 have been added after International Preliminary Examination.

This Preliminary Amendment also amends Claims 5-7, 10 and 16-17 so that these claims are no longer multiply dependent to reduce

Re: Preliminary Amendment  
August 14, 2001  
Page 8

the official fees at the U.S. Patent and Trademark Office (USPTO). The Applicants may elect to amend Claims 5-7, 10 and 16-17 to make them again multiply dependent or to add additional claims to this application to provide coverage similar to, broader than, or narrower than the present claims at any time during the pendency of the above-identified U.S. application.

Respectfully submitted,



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Enclosure: Appendix A (4 pages)

Appendix A

(VERSION WITH MARKINGS TO SHOW CHANGES MADE)

Page 1 of 4

1. (Amended) Computing apparatus comprising, mounted on an assembly, main processing means, [and] main memory means and a trusted device, each being connected for communication with one or more other components on the assembly, [characterised by further comprising a trusted device mounted on the assembly and being connected for communications with one or more other components on the assembly,] the trusted device being arranged to acquire a true value of an integrity metric of the computing apparatus.

4. (Amended) Computing apparatus according to claim 3, wherein the [platform] computing apparatus is arranged to cause the instructions to be the first instructions executed after release from reset.

5. (Amended) Computing apparatus according to claim 3 [or claim 4], wherein the trusted device is arranged to transfer the instructions to the main processing means in response to memory read signals from the main processing means.

6. (Amended) Computing apparatus according to [any one of claims 1 to 5] claim 1, wherein the trusted device comprises device memory means and is arranged to monitor [the] a data bus means by which components mounted on the assembly are adapted to communicate and store in the device memory means a flag in the event the first memory read signals generated by the main processing means after the computing apparatus is released from reset are addressed to the trusted device.

Appendix A

(VERSION WITH MARKINGS TO SHOW CHANGES MADE)

Page 2 of 4

7. (Amended) Computing apparatus according to [any one of claims 1 to 6]claim 1, wherein the trusted device has stored in device memory means at least one of:

- a unique identity of the trusted device;
- an authenticated integrity metric generated by a trusted party; and
- a secret.

10. (Amended) Computing apparatus according to claim 8 [or claim 9], wherein the trusted device has stored in device memory means an authenticated integrity metric generated by a trusted party and includes a encryption function, the trusted device being arranged to generate a response to a received challenge, the response comprising an acquired integrity metric and the authenticated integrity metric, both signed by the encryption function using the private asymmetric encryption key.

Please cancel claim 11 without prejudice.

## Appendix A

(VERSION WITH MARKINGS TO SHOW CHANGES MADE)

Page 3 of 4

12. (Amended) A method of operating a system comprising a trusted computing apparatus and a user, the trusted computing apparatus incorporating a trusted device being arranged to acquire the true value of an integrity metric of the trusted computing apparatus, the method comprising the steps of:

the trusted device acquiring the true value of the integrity metric of the trusted computing apparatus;

the user generating a challenge for the trusted computing apparatus to prove its integrity and submitting the challenge to the trusted computing apparatus;

the trusted computing apparatus receiving the challenge, and the trusted device generating a response including the integrity metric and returning the response to the user; and

the user receiving the response, extracting the integrity metric from the response and comparing the integrity metric with an authenticated metric for the trusted computing apparatus that had been generated by a trusted party.

16. (Amended) A method of establishing a communications channel in a system between trusted computing apparatus and remote computing apparatus, the method including the step of the remote computing apparatus verifying the integrity of the trusted computing apparatus using the method according to [any one of claims 12 to 15]claim 12, and maintaining the communications channel for further transactions in the event the integrity of the trusted computing apparatus is successfully verified by the remote computing apparatus.

Appendix A

(VERSION WITH MARKINGS TO SHOW CHANGES MADE)

Page 4 of 4

17. (Amended) A method of verifying that trusted computing apparatus is trustworthy for use by a user for processing a particular application, the method including the step of the user verifying the integrity of the trusted computing apparatus using the method according to [any one of claims]claim 12 [to 15], and the user using the trusted computing apparatus to process the particular application in the event the integrity of the trusted computing apparatus is successfully verified by the remote computing apparatus.

Please cancel claims 18-21 without prejudice.

5/PRTS

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533 Rec'd PCT/PTO 14 AUG 2001

09/913452

## Trusted Computing Platform

(HP Ref 30990050)

Technical Field

The present invention generally relates to trusted devices, trusted computing  
5 platforms, trusted transactions and methods of operating the same.

Background Art

For commercial applications, a client computing platform typically operates in an  
environment where its behaviour is vulnerable to modification by local or remote entities.  
10 This potential insecurity of the platform is a limitation on its use by local parties who might  
otherwise be willing to use the platform, or remote parties who might otherwise communicate  
with the platform; for example, for the purposes of E-commerce. For the present purposes,  
both local parties and remote parties will be referred to as "users" unless otherwise stated.

Existing security applications, for example virus detection software, execute on  
15 computing platforms under the assumption that the platform will operate as intended and  
that the platform will not subvert processes and applications. This is a valid assumption  
provided that the intended software state has not become unstable or has not been  
damaged by other software such as viruses. Users, therefore, typically restrict the use of  
such platforms to non-critical applications, and weigh the convenience of using the platforms  
20 against the risk to sensitive or business critical data.

Increasing the level of trust in platforms therefore enables greater user confidence in  
existing security applications (such as the 'Secure Sockets Layer' or 'IPSec') or remote  
management applications. This enables greater reliance on those applications and hence  
reduced 'cost of ownership'. Greater trust also enables new electronic methods of business,  
25 since there is greater confidence in the correct operation of both local and remote computing  
platforms.

In this document, the word 'trust' is used in the sense that something can be 'trusted'  
if it always behaves in the expected manner for the intended purpose.

30 Disclosure of the Invention

The present inventors have appreciated that it is desirable to use a physical device in  
a computing platform to verify and possibly enforce trust in that platform. Typically, the  
device provides trusted measurement and reporting of attributes of the associated platform,  
which indicate the integrity of the platform. Also, most preferably, the device is tamper-  
35 resistant.

In accordance with a first aspect, the present invention provides computing apparatus comprising, mounted on an assembly, main processing means and main memory means, each being connected for communication with one or more other components on the assembly, together with a trusted device mounted on the assembly and being connected for  
 5 communications with one or more other components on the assembly, the trusted device being arranged to acquire a true value of an integrity metric of the computing apparatus.

As used herein for reasons of simplicity of description, the term "device" also encompasses plural devices having equivalent function, or equivalent functionality integrated into one or more existing platform devices or assemblies. Additionally, the term 'true' as  
 10 used herein implies that the value is that which correctly reflects the state of the computing apparatus. This may be ensured if the measurement method is substantially un-modifiable other than by the trusted device.

In accordance with a second aspect, the present invention provides a method of operating a system comprising trusted computing apparatus and a user, the trusted  
 15 computing apparatus incorporating a trusted device being arranged to acquire the true value of an integrity metric of the computing apparatus, the method comprising the steps of:

the trusted device acquiring the true value of the integrity metric of the trusted computing apparatus;

the user generating a challenge for the trusted computing apparatus to prove its  
 20 integrity and submitting the challenge to the trusted computing apparatus;

the trusted computing apparatus receiving the challenge, and the trusted device generating a response including the integrity metric and returning the response to the user; and

the user receiving the response, extracting the integrity metric from the response and  
 25 comparing the integrity metric with an authenticated metric for the trusted computing apparatus that had been generated by a trusted party.

In accordance with a third aspect, the present invention provides a method of establishing a communications channel in a system between trusted computing apparatus and remote computing apparatus, the method including the step of the remote computing  
 30 apparatus verifying the integrity of the trusted computing apparatus using the above method, and maintaining the communications channel for further transactions in the event the integrity of the trusted computing apparatus is successfully verified by the remote computing apparatus.

In accordance with a fourth embodiment, the present invention provides a method of  
 35 verifying that trusted computing apparatus is trustworthy for use by a user for processing a

particular application, the method including the step of the user verifying the integrity of the trusted computing apparatus using the above method, and the user using the trusted computing apparatus to process the particular application in the event the integrity of the trusted computing apparatus is successfully verified by the remote computing apparatus.

5 Other aspects and embodiments of the present invention will become apparent from the following description and claims.

#### Brief Description of the Drawings

A preferred embodiment of the present invention will now be described by way of  
10 example only with reference to the accompanying drawings in which:

Figure 1 is a diagram that illustrates a system capable of implementing embodiments of the present invention;

Figure 2 is a diagram which illustrates a motherboard including a trusted device arranged to communicate with a smart card via a smart card reader and with a group of  
15 modules;

Figure 3 is a diagram that illustrates the trusted device in more detail;

Figure 4 is a flow diagram which illustrates the steps involved in acquiring an integrity metric of the computing apparatus;

Figure 5 is a flow diagram which illustrates the steps involved in establishing  
20 communications between a trusted computing platform and a remote platform including the trusted platform verifying its integrity; and

Figure 6 is a flow diagram which illustrates the steps involved in verification of a trusted computing platform by a potential user of that platform by means of a smart card.

#### 25 Best Mode For Carrying Out the Invention, & Industrial Applicability

The present exemplary embodiment generally provides the incorporation into a computing platform of a physical trusted device whose function is to bind the identity of the platform to reliably measured data that provides an integrity metric of the platform. The identity and the integrity metric are compared with expected values provided by a trusted  
30 party (TP) that is prepared to vouch for the trustworthiness of the platform. If there is a match, the implication is that at least part of the platform is operating correctly, depending on the scope of the integrity metric.

A user verifies the correct operation of the platform before exchanging other data with the platform. A user does this by requesting the trusted device to provide its identity  
35 and an integrity metric. (Optionally the trusted device will refuse to provide evidence of

identity if it itself was unable to verify correct operation of the platform.) The user receives the proof of identity and the identity metric, and compares them against values which it believes to be true. Those proper values are provided by the TP or another entity that is trusted by the user. If data reported by the trusted device is the same as that provided by the TP, the user trusts the platform. This is because the user trusts the entity. The entity trusts the platform because it has previously validated the identity and determined the proper integrity metric of the platform.

Once a user has established trusted operation of the platform, he exchanges other data with the platform. For a local user, the exchange might be by interacting with some software application running on the platform. For a remote user, the exchange might involve a secure transaction. In either case, the data exchanged is 'signed' by the trusted device. The user can then have greater confidence that data is being exchanged with a platform whose behaviour can be trusted.

The trusted device uses cryptographic processes but does not necessarily provide an external interface to those cryptographic processes. Also, a most desirable implementation would be to make the trusted device tamperproof, to protect secrets by making them inaccessible to other platform functions and provide an environment that is substantially immune to unauthorised modification. Since tamper-proofing is impossible, the best approximation is a trusted device that is tamper-resistant, or tamper-detecting. The trusted device, therefore, preferably consists of one physical component that is tamper-resistant.

Techniques relevant to tamper-resistance are well known to those skilled in the art of security. These techniques include methods for resisting tampering (such as appropriate encapsulation of the trusted device), methods for detecting tampering (such as detection of out of specification voltages, X-rays, or loss of physical integrity in the trusted device casing), and methods for eliminating data when tampering is detected. Further discussion of appropriate techniques can be found at <http://www.cl.cam.ac.uk/~mgk25/tamper.html>. It will be appreciated that, although tamper-proofing is a most desirable feature of the present invention, it does not enter into the normal operation of the invention and, as such, is beyond the scope of the present invention and will not be described in any detail herein.

The trusted device is preferably a physical one because it must be difficult to forge. It is most preferably tamper-resistant because it must be hard to counterfeit. It typically has an engine capable of using cryptographic processes because it is required to prove identity, both locally and at a distance, and it contains at least one method of measuring some integrity metric of the platform with which it is associated.

A trusted platform 10 is illustrated in the diagram in Figure 1. The platform 10 includes the standard features of a keyboard 14, mouse 16 and visual display unit (VDU) 18, which provide the physical 'user interface' of the platform. This embodiment of a trusted platform also contains a smart card reader 12 - a smart card reader is not an essential  
 5 element of all trusted platforms, but is employed in various preferred embodiments described below. Along side the smart card reader 12, there is illustrated a smart card 19 to allow trusted user interaction with the trusted platform as shall be described further below. In the platform 10, there are a plurality of modules 15: these are other functional elements of the trusted platform of essentially any kind appropriate to that platform (the functional  
 10 significance of such elements is not relevant to the present invention and will not be discussed further herein).

As illustrated in Figure 2, the motherboard 20 of the trusted computing platform 10 includes (among other standard components) a main processor 21, main memory 22, a trusted device 24, a data bus 26 and respective control lines 27 and lines 28, BIOS memory  
 15 29 containing the BIOS program for the platform 10 and an Input/Output (IO) device 23, which controls interaction between the components of the motherboard and the smart card reader 12, the keyboard 14, the mouse 16 and the VDU 18. The main memory 22 is typically random access memory (RAM). In operation, the platform 10 loads the operating system, for example Windows NT™, into RAM from hard disk (not shown). Additionally, in  
 20 operation, the platform 10 loads the processes or applications that may be executed by the platform 10 into RAM from hard disk (not shown).

Typically, in a personal computer the BIOS program is located in a special reserved memory area, the upper 64K of the first megabyte of the system memory (addresses F000h to FFFFh), and the main processor is arranged to look at this memory location first,  
 25 in accordance with an industry wide standard.

The significant difference between the platform and a conventional platform is that, after reset, the main processor is initially controlled by the trusted device, which then hands control over to the platform-specific BIOS program, which in turn initialises all input/output devices as normal. After the BIOS program has executed, control is handed over as normal  
 30 by the BIOS program to an operating system program, such as Windows NT (TM), which is typically loaded into main memory 22 from a hard disk drive (not shown).

Clearly, this change from the normal procedure requires a modification to the implementation of the industry standard, whereby the main processor 21 is directed to address the trusted device 24 to receive its first instructions. This change may be made  
 35 simply by hard-coding a different address into the main processor 21. Alternatively, the

trusted device 24 may be assigned the standard BIOS program address, in which case there is no need to modify the main processor configuration.

It is highly desirable for the BIOS boot block to be contained within the trusted device 24. This prevents subversion of the obtaining of the integrity metric (which could otherwise occur if rogue software processes are present) and prevents rogue software processes creating a situation in which the BIOS (even if correct) fails to build the proper environment for the operating system.

Although, in the preferred embodiment to be described, the trusted device 24 is a single, discrete component, it is envisaged that the functions of the trusted device 24 may alternatively be split into multiple devices on the motherboard, or even integrated into one or more of the existing standard devices of the platform. For example, it is feasible to integrate one or more of the functions of the trusted device into the main processor itself, provided that the functions and their communications cannot be subverted. This, however, would probably require separate leads on the processor for sole use by the trusted functions. Additionally or alternatively, although in the present embodiment the trusted device is a hardware device that is adapted for integration into the motherboard 20, it is anticipated that a trusted device may be implemented as a 'removable' device, such as a dongle, which could be attached to a platform when required. Whether the trusted device is integrated or removable is a matter of design choice. However, where the trusted device is separable, a mechanism for providing a logical binding between the trusted device and the platform should be present.

The trusted device 24 comprises a number of blocks, as illustrated in Figure 3. After system reset, the trusted device 24 performs a secure boot process to ensure that the operating system of the platform 10 (including the system clock and the display on the monitor) is running properly and in a secure manner. During the secure boot process, the trusted device 24 acquires an integrity metric of the computing platform 10. The trusted device 24 can also perform secure data transfer and, for example, authentication between it and a smart card via encryption/decryption and signature/verification. The trusted device 24 can also securely enforce various security control policies, such as locking of the user interface.

Specifically, the trusted device comprises: a controller 30 programmed to control the overall operation of the trusted device 24, and interact with the other functions on the trusted device 24 and with the other devices on the motherboard 20; a measurement function 31 for acquiring the integrity metric from the platform 10; a cryptographic function 32 for signing, encrypting or decrypting specified data; an authentication function 33 for authenticating a

smart card; and interface circuitry 34 having appropriate ports (36, 37 & 38) for connecting the trusted device 24 respectively to the data bus 26, control lines 27 and address lines 28 of the motherboard 20. Each of the blocks in the trusted device 24 has access (typically via the controller 30) to appropriate volatile memory areas 4 and/or non-volatile memory areas 3 of the trusted device 24. Additionally, the trusted device 24 is designed, in a known manner, to be tamper resistant.

For reasons of performance, the trusted device 24 may be implemented as an application specific integrated circuit (ASIC). However, for flexibility, the trusted device 24 is preferably an appropriately programmed micro-controller. Both ASICs and micro-controllers are well known in the art of microelectronics and will not be considered herein in any further detail.

One item of data stored in the non-volatile memory 3 of the trusted device 24 is a certificate 350. The certificate 350 contains at least a public key 351 of the trusted device 24 and an authenticated value 352 of the platform integrity metric measured by a trusted party (TP). The certificate 350 is signed by the TP using the TP's private key prior to it being stored in the trusted device 24. In later communications sessions, a user of the platform 10 can verify the integrity of the platform 10 by comparing the acquired integrity metric with the authentic integrity metric 352. If there is a match, the user can be confident that the platform 10 has not been subverted. Knowledge of the TP's generally-available public key enables simple verification of the certificate 350. The non-volatile memory 35 also contains an identity (ID) label 353. The ID label 353 is a conventional ID label, for example a serial number, that is unique within some context. The ID label 353 is generally used for indexing and labelling of data relevant to the trusted device 24, but is insufficient in itself to prove the identity of the platform 10 under trusted conditions.

The trusted device 24 is equipped with at least one method of reliably measuring or acquiring the integrity metric of the computing platform 10 with which it is associated. In the present embodiment, the integrity metric is acquired by the measurement function 31 by generating a digest of the BIOS instructions in the BIOS memory. Such an acquired integrity metric, if verified as described above, gives a potential user of the platform 10 a high level of confidence that the platform 10 has not been subverted at a hardware, or BIOS program, level. Other known processes, for example virus checkers, will typically be in place to check that the operating system and application program code has not been subverted.

The measurement function 31 has access to: non-volatile memory 3 for storing a hash program 354 and a private key 355 of the trusted device 24, and volatile memory 4 for storing acquired integrity metric in the form of a digest 361. In appropriate embodiments, the

volatile memory 4 may also be used to store the public keys and associated ID labels 360a-360n of one or more authentic smart cards 19s that can be used to gain access to the platform 10.

In one preferred implementation, as well as the digest, the integrity metric includes a Boolean value, which is stored in volatile memory 4 by the measurement function 31, for reasons that will become apparent.

A preferred process for acquiring an integrity metric will now be described with reference to Figure 4.

In step 500, at switch-on, the measurement function 31 monitors the activity of the main processor 21 on the data, control and address lines (26, 27 & 28) to determine whether the trusted device 24 is the first memory accessed. Under conventional operation, a main processor would first be directed to the BIOS memory first in order to execute the BIOS program. However, in accordance with the present embodiment, the main processor 21 is directed to the trusted device 24, which acts as a memory. In step 505, if the trusted device 24 is the first memory accessed, in step 510, the measurement function 31 writes to volatile memory 3 a Boolean value which indicates that the trusted device 24 was the first memory accessed. Otherwise, in step 515, the measurement function writes a Boolean value which indicates that the trusted device 24 was not the first memory accessed.

In the event the trusted device 24 is not the first accessed, there is of course a chance that the trusted device 24 will not be accessed at all. This would be the case, for example, if the main processor 21 were manipulated to run the BIOS program first. Under these circumstances, the platform would operate, but would be unable to verify its integrity on demand, since the integrity metric would not be available. Further, if the trusted device 24 were accessed after the BIOS program had been accessed, the Boolean value would clearly indicate lack of integrity of the platform.

In step 520, when (or if) accessed as a memory by the main processor 21, the main processor 21 reads the stored native hash instructions 354 from the measurement function 31 in step 525. The hash instructions 354 are passed for processing by the main processor 21 over the data bus 26. In step 530, main processor 21 executes the hash instructions 354 and uses them, in step 535, to compute a digest of the BIOS memory 29, by reading the contents of the BIOS memory 29 and processing those contents according to the hash program. In step 540, the main processor 21 writes the computed digest 361 to the appropriate non-volatile memory location 4 in the trusted device 24. The measurement function 31, in step 545, then calls the BIOS program in the BIOS memory 29, and execution continues in a conventional manner.

Clearly, there are a number of different ways in which the integrity metric may be calculated, depending upon the scope of the trust required. The measurement of the BIOS program's integrity provides a fundamental check on the integrity of a platform's underlying processing environment. The integrity metric should be of such a form that it will enable reasoning about the validity of the boot process - the value of the integrity metric can be used to verify whether the platform booted using the correct BIOS. Optionally, individual functional blocks within the BIOS could have their own digest values, with an ensemble BIOS digest being a digest of these individual digests. This enables a policy to state which parts of BIOS operation are critical for an intended purpose, and which are irrelevant (in which case the individual digests must be stored in such a manner that validity of operation under the policy can be established).

Other integrity checks could involve establishing that various other devices, components or apparatus attached to the platform are present and in correct working order. In one example, the BIOS programs associated with a SCSI controller could be verified to ensure communications with peripheral equipment could be trusted. In another example, the integrity of other devices, for example memory devices or co-processors, on the platform could be verified by enacting fixed challenge/response interactions to ensure consistent results. Where the trusted device is a separable component, some such form of interaction is desirable to provide an appropriate logical binding between the trusted device and the platform. Also, although in the present embodiment the trusted device utilises the data bus as its main means of communication with other parts of the platform, it would be feasible, although not so convenient, to provide alternative communications paths, such as hard-wired paths or optical paths. Further, although in the present embodiment the trusted device instructs the main processor to calculate the integrity metric in other embodiments, the trusted device itself is arranged to measure one or more integrity metrics.

Preferably, the BIOS boot process includes mechanisms to verify the integrity of the boot process itself. Such mechanisms are already known from, for example, Intel's draft "Wired for Management baseline specification v 2.0 - BOOT Integrity Service", and involve calculating digests of software or firmware before loading that software or firmware. Such a computed digest is compared with a value stored in a certificate provided by a trusted entity, whose public key is known to the BIOS. The software/firmware is then loaded only if the computed value matches the expected value from the certificate, and the certificate has been proven valid by use of the trusted entity's public key. Otherwise, an appropriate exception handling routine is invoked.

Optionally, after receiving the computed BIOS digest, the trusted device 24 may inspect the proper value of the BIOS digest in the certificate and not pass control to the BIOS if the computed digest does not match the proper value. Additionally, or alternatively, the trusted device 24 may inspect the Boolean value and not pass control back to the BIOS if the trusted device 24 was not the first memory accessed. In either of these cases, an appropriate exception handling routine may be invoked.

Figure 5 illustrates the flow of actions by a TP, the trusted device 24 incorporated into a platform, and a user (of a remote platform) who wants to verify the integrity of the trusted platform. It will be appreciated that substantially the same steps as are depicted in Figure 5 are involved when the user is a local user. In either case, the user would typically rely on some form of software application to enact the verification. It would be possible to run the software application on the remote platform or the trusted platform. However, there is a chance that, even on the remote platform, the software application could be subverted in some way. Therefore, it is anticipated that, for a high level of integrity, the software application would reside on a smart card of the user, who would insert the smart card into an appropriate reader for the purposes of verification. Figure 5 illustrates the flow of actions for the general case - a more specific flow of actions for verification by a user smart card will be described with reference to Figure 6 further below.

At the first instance, a TP, which vouches for trusted platforms, will inspect the type of the platform to decide whether to vouch for it or not. This will be a matter of policy. If all is well, in step 600, the TP measures the value of integrity metric of the platform. Then, the TP generates a certificate, in step 605, for the platform. The certificate is generated by the TP by appending the trusted device's public key, and optionally its ID label, to the measured integrity metric, and signing the string with the TP's private key.

The trusted device 24 can subsequently prove its identity by using its private key to process some input data received from the user and produce output data, such that the input/output pair is statistically impossible to produce without knowledge of the private key. Hence, knowledge of the private key forms the basis of identity in this case. Clearly, it would be feasible to use symmetric encryption to form the basis of identity. However, the disadvantage of using symmetric encryption is that the user would need to share his secret with the trusted device. Further, as a result of the need to share the secret with the user, while symmetric encryption would in principle be sufficient to prove identity to the user, it would be insufficient to prove identity to a third party, who could not be entirely sure the verification originated from the trusted device or the user.

In step 610, the trusted device 24 is initialised by writing the certificate 350 into the appropriate non-volatile memory locations 3 of the trusted device 24. This is done, preferably, by secure communication with the trusted device 24 after it is installed in the motherboard 20. The method of writing the certificate to the trusted device 24 is analogous  
 5 to the method used to initialise smart cards by writing private keys thereto. The secure communications is supported by a 'master key', known only to the TP, that is written to the trusted device (or smart card) during manufacture, and used to enable the writing of data to the trusted device 24; writing of data to the trusted device 24 without knowledge of the master key is not possible.

10 At some later point during operation of the platform, for example when it is switched on or reset, in step 615, the trusted device 24 acquires and stores the integrity metric 361 of the platform.

When a user wishes to communicate with the platform, in step 620, he creates a nonce, such as a random number, and, in step 625, challenges the trusted device 24 (the  
 15 operating system of the platform, or an appropriate software application, is arranged to recognise the challenge and pass it to the trusted device 24, typically via a BIOS-type call, in an appropriate fashion). The nonce is used to protect the user from deception caused by replay of old but genuine signatures (called a 'replay attack') by untrustworthy platforms. The process of providing a nonce and verifying the response is an example of the well-  
 20 known 'challenge/response' process.

In step 630, the trusted device 24 receives the challenge and creates an appropriate response. This may be a digest of the measured integrity metric and the nonce, and optionally its ID label. Then, in step 635, the trusted device 24 signs the digest, using its private key, and returns the signed digest, accompanied by the certificate 350, to the user.

25 In step 640, the user receives the challenge response and verifies the certificate using the well known public key of the TP. The user then, in step 650, extracts the trusted device's 24 public key from the certificate and uses it to decrypt the signed digest from the challenge response. Then, in step 660, the user verifies the nonce inside the challenge response. Next, in step 670, the user compares the computed integrity metric, which it  
 30 extracts from the challenge response, with the proper platform integrity metric, which it extracts from the certificate. If any of the foregoing verification steps fails, in steps 645, 655, 665 or 675, the whole process ends in step 680 with no further communications taking place.

Assuming all is well, in steps 685 and 690, the user and the trusted platform use other protocols to set up secure communications for other data, where the data from the  
 35 platform is preferably signed by the trusted device 24.

Further refinements of this verification process are possible. It is desirable that the challenger becomes aware, through the challenge, both of the value of the platform integrity metric and also of the method by which it was obtained. Both these pieces of information are desirable to allow the challenger to make a proper decision about the integrity of the platform. The challenger also has many different options available - it may accept that the integrity metric is recognised as valid in the trusted device 24, or may alternatively only accept that the platform has the relevant level of integrity if the value of the integrity metric is equal to a value held by the challenger (or may hold there to be different levels of trust in these two cases).

10 The techniques of signing, using certificates, and challenge/response, and using them to prove identity, are well known to those skilled in the art of security and therefore need not be described in any more detail herein.

As indicated above, Figure 6 shows the flow of actions in an example of verification of platform integrity by a user interacting with the trusted platform with a smart card 19. As will be described, the process conveniently implements a challenge/response routine. There exist many available challenge/response mechanisms. The implementation of an authentication protocol used in the present embodiment is mutual (or 3-step) authentication, as described in ISO/IEC 9798-3, "Information technology – Security techniques – Entity authentication mechanisms; Part 3; Entity authentication using a public key algorithm", 20 International Organization for Standardization, November 1993. Of course, there is no reason why other authentication procedures cannot be used, for example 2-step or 4-step, as also described in this reference.

Initially, the user inserts their smart card 19 into the smart card reader 12 of the platform in step 700.

25 Beforehand, a platform configured for use by users of in this way will typically be operating under the control of its standard operating system and executing the authentication process, which waits for a user to insert their smart card 19. Apart from the smart card reader 12 being active in this way, such a platform is typically rendered inaccessible to users by 'locking' the user interface (i.e. the screen, keyboard and mouse). 30 This will however not be the case in all embodiments of the invention.

When the smart card 19 is inserted into the smart card reader 12, the trusted device 24 is triggered to attempt mutual authentication in step by generating and transmitting a nonce A to the smart card 19 in step 705. A nonce, such as a random number, is used to protect the originator from deception caused by replay of old but genuine responses (called 35 a 'replay attack') by untrustworthy third parties.

In response, in step 710, the smart card 19 generates and returns a response comprising the concatenation of: the plain text of the nonce A, a new nonce B generated by the smart card 19, an ID of the trusted device 24 and some redundancy; the signature of the plain text, generated by signing the plain text with the private key of the smart card 19; and a  
5 certificate containing the ID and the public key of the smart card 19.

The trusted device 24 authenticates the response by using the public key in the certificate to verify the signature of the plain text in step 715. If the response is not authentic, the process ends in step 720. If the response is authentic, in step 725 the trusted device 24 generates and sends a further response including the concatenation of: the plain  
10 text of the nonce A, the nonce B, an ID of the smart card 19 and the acquired integrity metric; the signature of the plain text, generated by signing the plain text using the private key of the trusted device 24; and the certificate comprising the public key of the trusted device 24 and the authentic integrity metric, both signed by the private key of the TP.

The smart card 19 authenticates this response by using the public key of the TP and  
15 comparing the acquired integrity metric with the authentic integrity metric, where a match indicates successful verification, in step 730. If the further response is not authentic, the process ends in step 735.

If the procedure is successful, both the trusted device 24 has authenticated the logon card 19 and the smart card 19 has verified the integrity of the trusted platform and, in step  
20 740, the authentication process executes the secure process for the user.

In certain types of interaction, the authentication process can end at this point. However, if a session is to be continued between the user and the trusted platform, it is desirable to ensure that the user remains authenticated to the platform.

Where continued authentication is required, the authentication process sets an  
25 interval timer in step 745. Thereafter, using appropriate operating system interrupt routines, the authentication process services the interval timer periodically to detect when the timer meets or exceeds a pre-determined timeout period in step 750.

Clearly, the authentication process and the interval timer run in parallel with the secure process. When the timeout period is met or exceeded, the authentication process  
30 triggers the trusted device 24 to re-authenticate the smart card 19, by transmitting a challenge for the smart card 19 to identify itself in step 760. The smart card 19 returns a certificate including its ID and its public key in step 765. In step 770, if there is no response (for example, as a result of the smart card 19 having been removed) or the certificate is no longer valid for some reason (for example, the smart card has been replaced with a different

smart card), the session is terminated by the trusted device 24 in step 775. Otherwise, in step 770, the process from step 745 repeats by resetting the interval timer.

Additionally, or alternatively, in some embodiments it may be required that the user profile is encrypted and signed to protect privacy and integrity. If so, a secure data transfer protocol may be needed between the trusted device 24 and the smart card 19. There exist many available mechanisms for transferring secure credentials between two entities. A possible implementation, which may be used in the present embodiment, is secure key transport mechanisms from ISO/IEC DIS 11770-3, "Information technology – Security techniques – Key management - Part 3: Mechanisms using asymmetric techniques", International Organization for Standardization, March 1997.

Modifications of this verification process using other well-known challenge and response techniques can easily be achieved by the skilled person. Similarly, alternative verification processes can be used by parties interacting with the platform in a different manner (that is, other than as a user equipped with a smart card).

## CLAIMS

30990050

1. Computing apparatus comprising mounted on an assembly main processing means and  
5 main memory means, each being connected for communication with one or more other components on the assembly,

characterised by further comprising a trusted device mounted on the assembly and being connected for communications with one or more other components on the assembly, the trusted device being arranged to acquire a true value of an integrity metric of the  
10 computing apparatus.

2. Computing apparatus according to claim 1, wherein the trusted device comprises device memory means and means for instructing the main processing means to determine the integrity metric and return the integrity metric for storage in the device memory means.

3. Computing apparatus according to claim 2, wherein the means for instructing the main processing means comprises, stored in the device memory means, program code native to the main processing means, and the trusted device is arranged to transfer the instructions of the program code to the main processing means.

4. Computing apparatus according to claim 3, wherein the platform is arranged to cause the instructions to be the first instructions executed after release from reset.

5. Computing apparatus according to claim 3 or claim 4, wherein the trusted device is  
25 arranged to transfer the instructions to the main processing means in response to memory read signals from the main processing means.

6. Computing apparatus according to any one of claims 1 to 5, wherein the trusted device comprises device memory means and is arranged to monitor the data bus means and store  
30 in the device memory means a flag in the event the first memory read signals generated by the main processing means after the computing apparatus is released from reset are addressed to the trusted device.

7. Computing apparatus according to any one of claims 1 to 6, wherein the trusted device has stored in device memory means at least one of:

- a unique identity of the trusted device;
- an authenticated integrity metric generated by a trusted party; and
- 5 a secret.

8. Computing apparatus according to claim 7, wherein the trusted device has stored in device memory means a secret comprising a private asymmetric encryption key.

10 9. Computing apparatus according to claim 8, wherein the trusted device also has stored in device memory means a respective public encryption key that has been signed by a trusted party.

10. Computing apparatus according to claim 8 or claim 9, wherein the trusted device has  
15 stored in device memory means an authenticated integrity metric generated by a trusted party and includes a encryption function, the trusted device being arranged to generate a response to a received challenge, the response comprising an acquired integrity metric and the authenticated integrity metric, both signed by the encryption function using the private asymmetric encryption key.

20

11. A trusted device configured for use in computing apparatus according to any one of the preceding claims.

12. A method of operating a system comprising trusted computing apparatus and a user,  
25 the trusted computing apparatus incorporating a trusted device being arranged to acquire the true value of an integrity metric of the computing apparatus, the method comprising the steps of:

- the trusted device acquiring the true value of the integrity metric of the trusted computing apparatus;

30 the user generating a challenge for the trusted computing apparatus to prove its integrity and submitting the challenge to the trusted computing apparatus;

- the trusted computing apparatus receiving the challenge, and the trusted device generating a response including the integrity metric and returning the response to the user; and

the user receiving the response, extracting the integrity metric from the response and comparing the integrity metric with an authenticated metric for the trusted computing apparatus that had been generated by a trusted party.

5 13. A method according to claim 12, wherein the challenge includes a nonce, the response includes the integrity metric and the nonce, both digitally signed by the trusted device using a information security algorithm, and the user verifies the integrity metric and the nonce using a respective information security algorithm.

10 14. A method according to claim 13, wherein the trusted device uses a private encryption key to sign the integrity metric and the nonce, and the user uses the respective public encryption key to verify the integrity metric and the nonce.

15 15. A method according to claim 14, wherein the response includes a certificate held by the trusted device, which certificate has been digitally signed by a trusted party using a private encryption key of the trusted party, the certificate including the public encryption key of the trusted device, and the user verifies the certificate using the public encryption key of the trusted party and uses the public encryption key from the certificate to verify the integrity metric and the nonce.

20

16. A method of establishing a communications channel in a system between trusted computing apparatus and remote computing apparatus, the method including the step of the remote computing apparatus verifying the integrity of the trusted computing apparatus using the method according to any one of claims 12 to 15, and maintaining the communications  
25 channel for further transactions in the event the integrity of the trusted computing apparatus is successfully verified by the remote computing apparatus.

17. A method of verifying that trusted computing apparatus is trustworthy for use by a user for processing a particular application, the method including the step of the user verifying the  
30 integrity of the trusted computing apparatus using the method according to any one of claims 12 to 15, and the user using the trusted computing apparatus to process the particular application in the event the integrity of the trusted computing apparatus is successfully verified by the remote computing apparatus.

18. Trusted computing apparatus adapted for use in accordance with the method of any one of claims 12 to 17.

19. Remote computing apparatus arranged for use in accordance with claim 16.

5

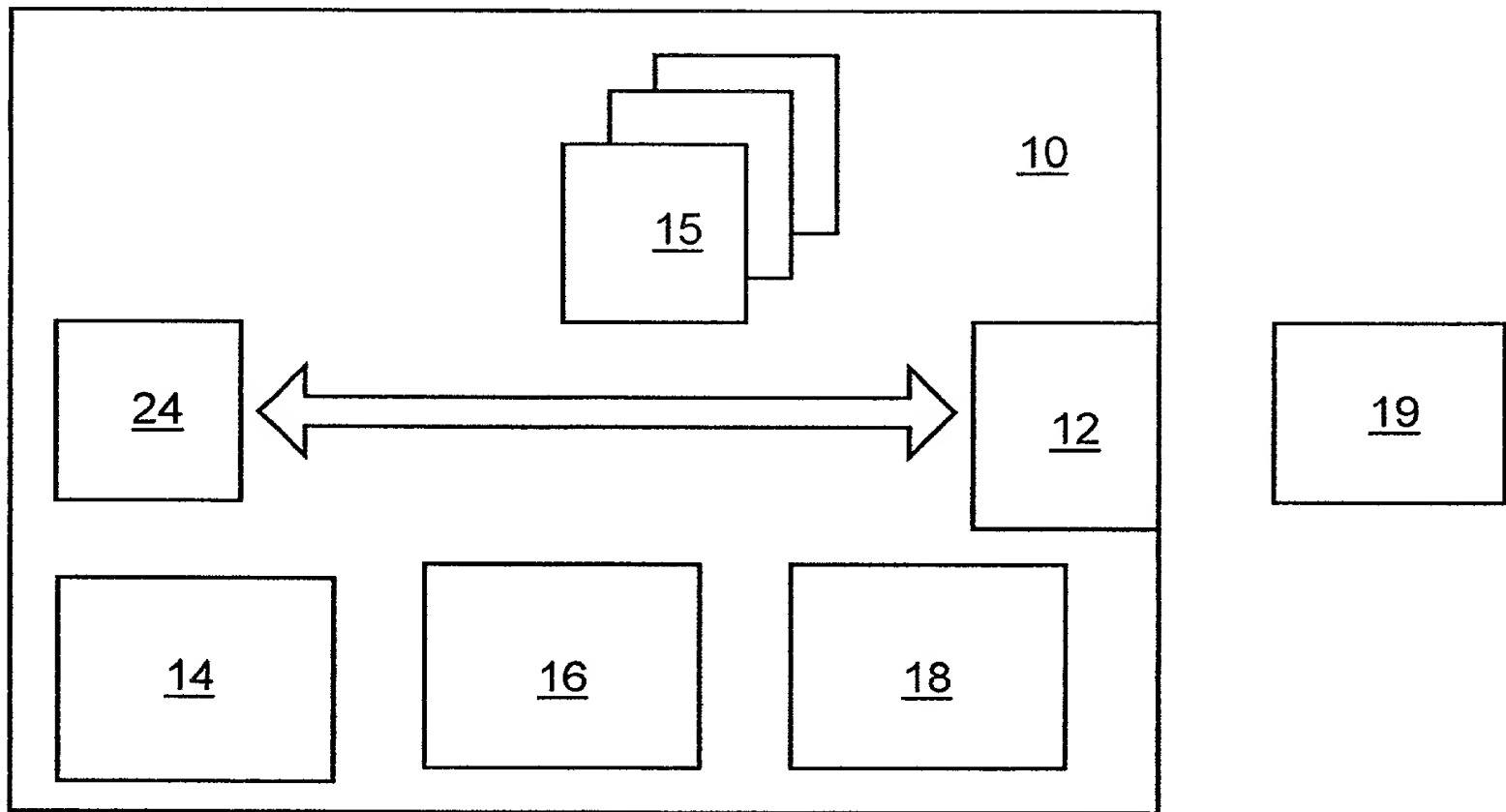
20. A trusted device arranged for use in accordance with any one of claims 12 to 17.

21. Computing apparatus configured to receive a trusted device as claimed in claim 11.

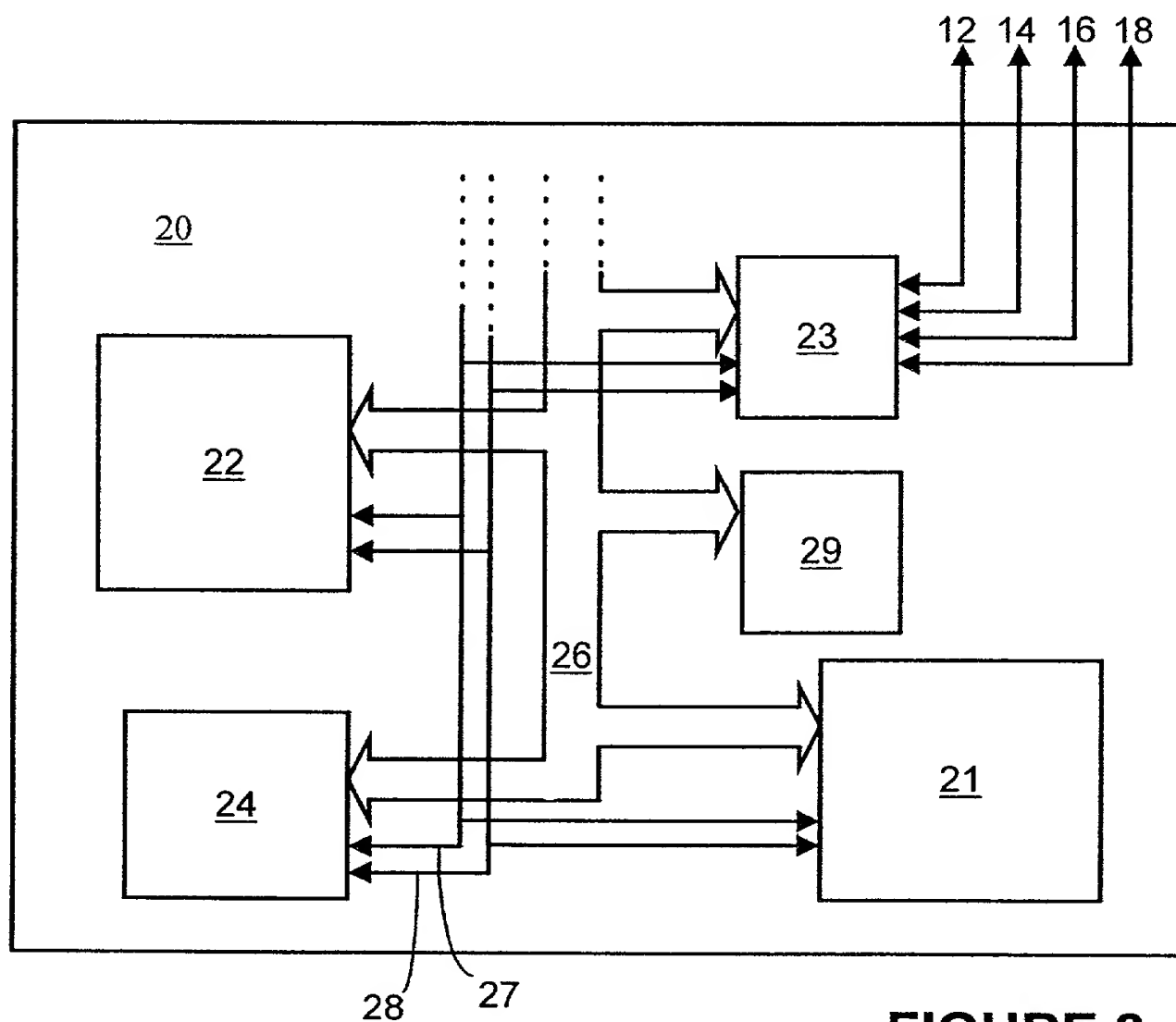
10

Year	Total population		Male		Female		Total population	Male		Female		
	Population	%	Population	%	Population	%		Population	%	Population	%	
1950	1,000,000	100	500,000	50	500,000	50	1,000,000	100	500,000	50	500,000	50
1951	1,010,000	101	505,000	50	505,000	50	1,010,000	101	505,000	50	505,000	50
1952	1,020,000	102	510,000	50	510,000	50	1,020,000	102	510,000	50	510,000	50
1953	1,030,000	103	515,000	50	515,000	50	1,030,000	103	515,000	50	515,000	50
1954	1,040,000	104	520,000	50	520,000	50	1,040,000	104	520,000	50	520,000	50
1955	1,050,000	105	525,000	50	525,000	50	1,050,000	105	525,000	50	525,000	50
1956	1,060,000	106	530,000	50	530,000	50	1,060,000	106	530,000	50	530,000	50
1957	1,070,000	107	535,000	50	535,000	50	1,070,000	107	535,000	50	535,000	50
1958	1,080,000	108	540,000	50	540,000	50	1,080,000	108	540,000	50	540,000	50
1959	1,090,000	109	545,000	50	545,000	50	1,090,000	109	545,000	50	545,000	50
1960	1,100,000	110	550,000	50	550,000	50	1,100,000	110	550,000	50	550,000	50
1961	1,110,000	111	555,000	50	555,000	50	1,110,000	111	555,000	50	555,000	50
1962	1,120,000	112	560,000	50	560,000	50	1,120,000	112	560,000	50	560,000	50
1963	1,130,000	113	565,000	50	565,000	50	1,130,000	113	565,000	50	565,000	50
1964	1,140,000	114	570,000	50	570,000	50	1,140,000	114	570,000	50	570,000	50
1965	1,150,000	115	575,000	50	575,000	50	1,150,000	115	575,000	50	575,000	50
1966	1,160,000	116	580,000	50	580,000	50	1,160,000	116	580,000	50	580,000	50
1967	1,170,000	117	585,000	50	585,000	50	1,170,000	117	585,000	50	585,000	50
1968	1,180,000	118	590,000	50	590,000	50	1,180,000	118	590,000	50	590,000	50
1969	1,190,000	119	595,000	50	595,000	50	1,190,000	119	595,000	50	595,000	50
1970	1,200,000	120	600,000	50	600,000	50	1,200,000	120	600,000	50	600,000	50
1971	1,210,000	121	605,000	50	605,000	50	1,210,000	121	605,000	50	605,000	50
1972	1,220,000	122	610,000	50	610,000	50	1,220,000	122	610,000	50	610,000	50
1973	1,230,000	123	615,000	50	615,000	50	1,230,000	123	615,000	50	615,000	50
1974	1,240,000	124	620,000	50	620,000	50	1,240,000	124	620,000	50	620,000	50
1975	1,250,000	125	625,000	50	625,000	50	1,250,000	125	625,000	50	625,000	50
1976	1,260,000	126	630,000	50</								

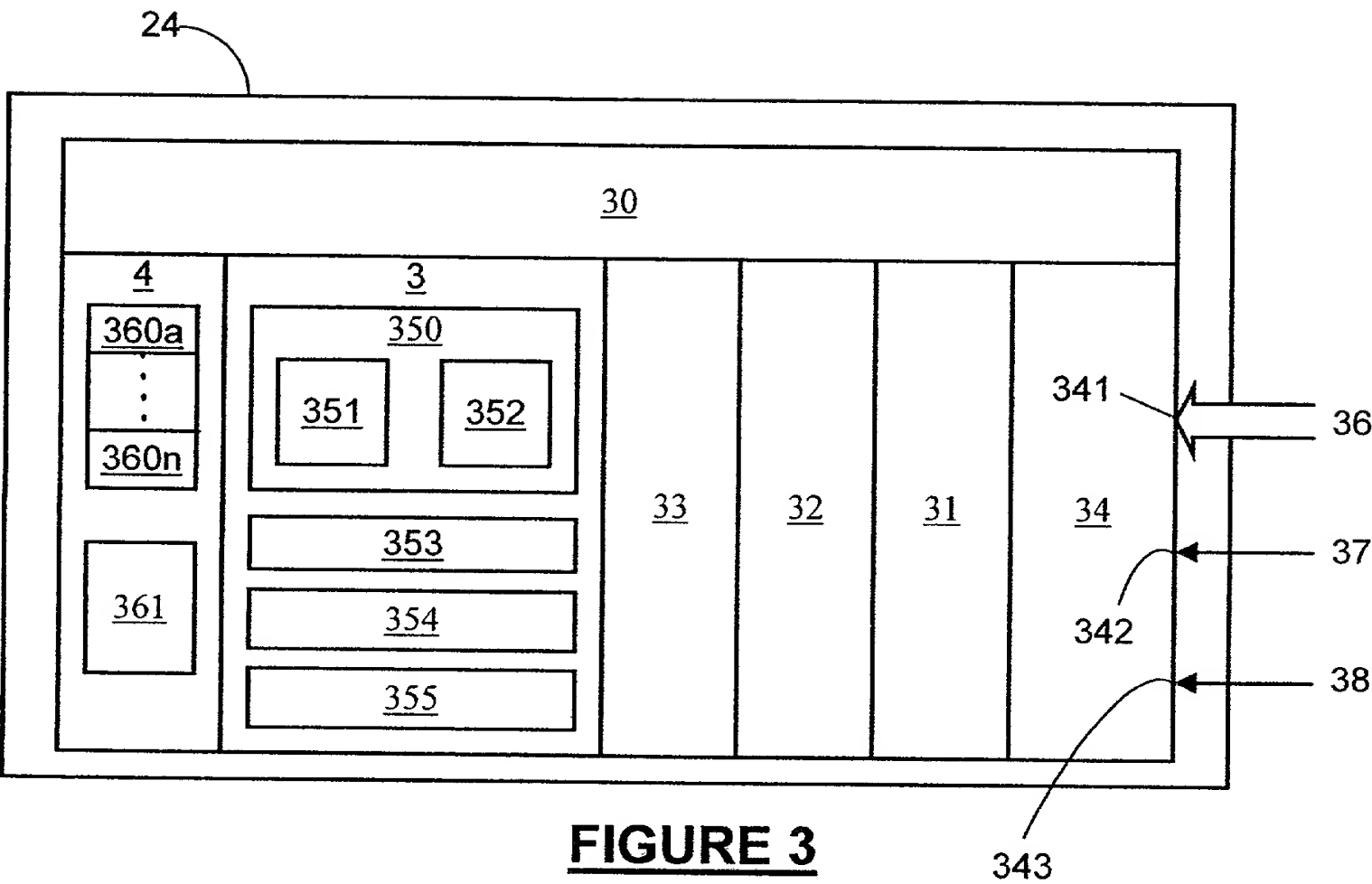
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**FIGURE 1**

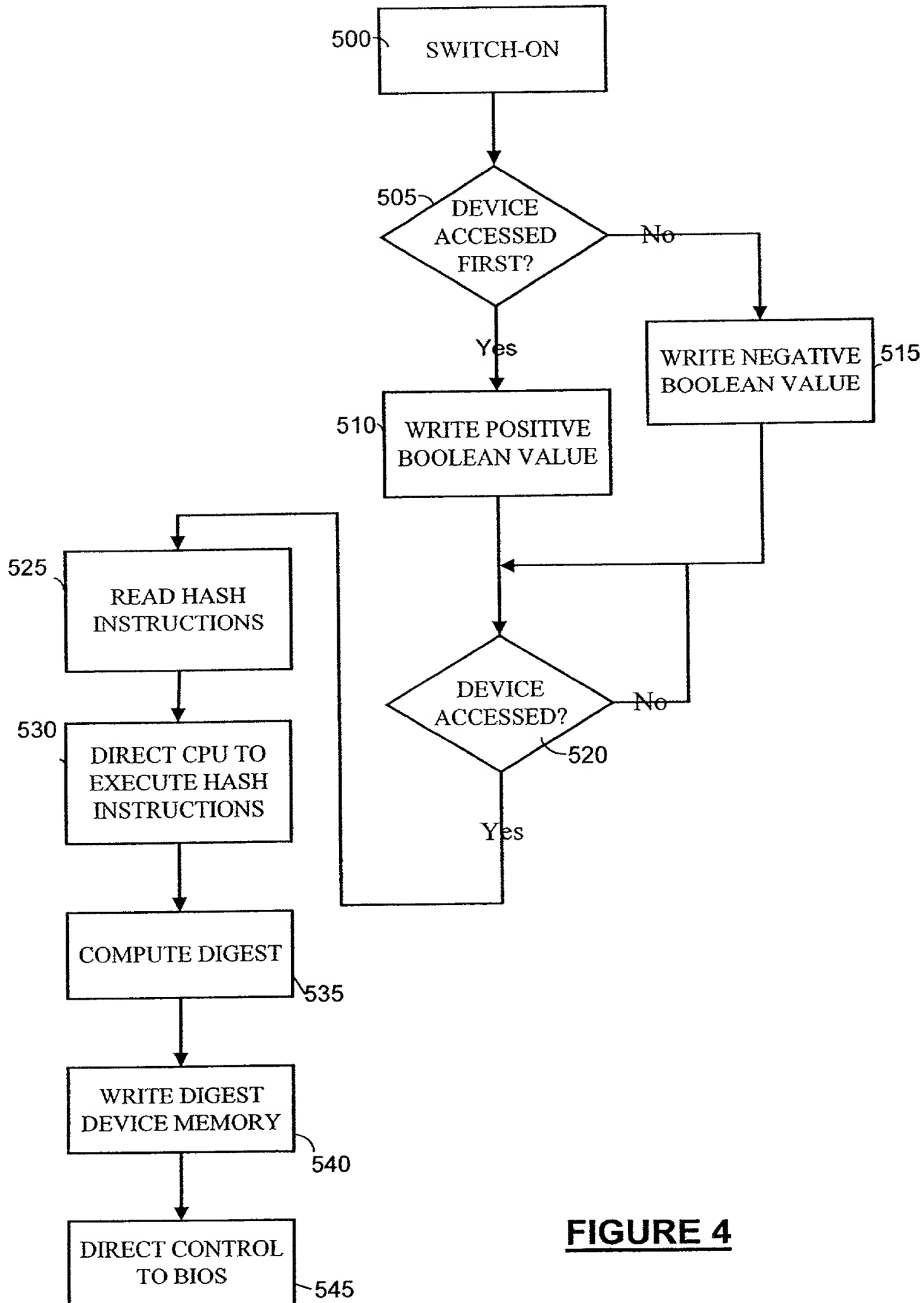


**FIGURE 2**

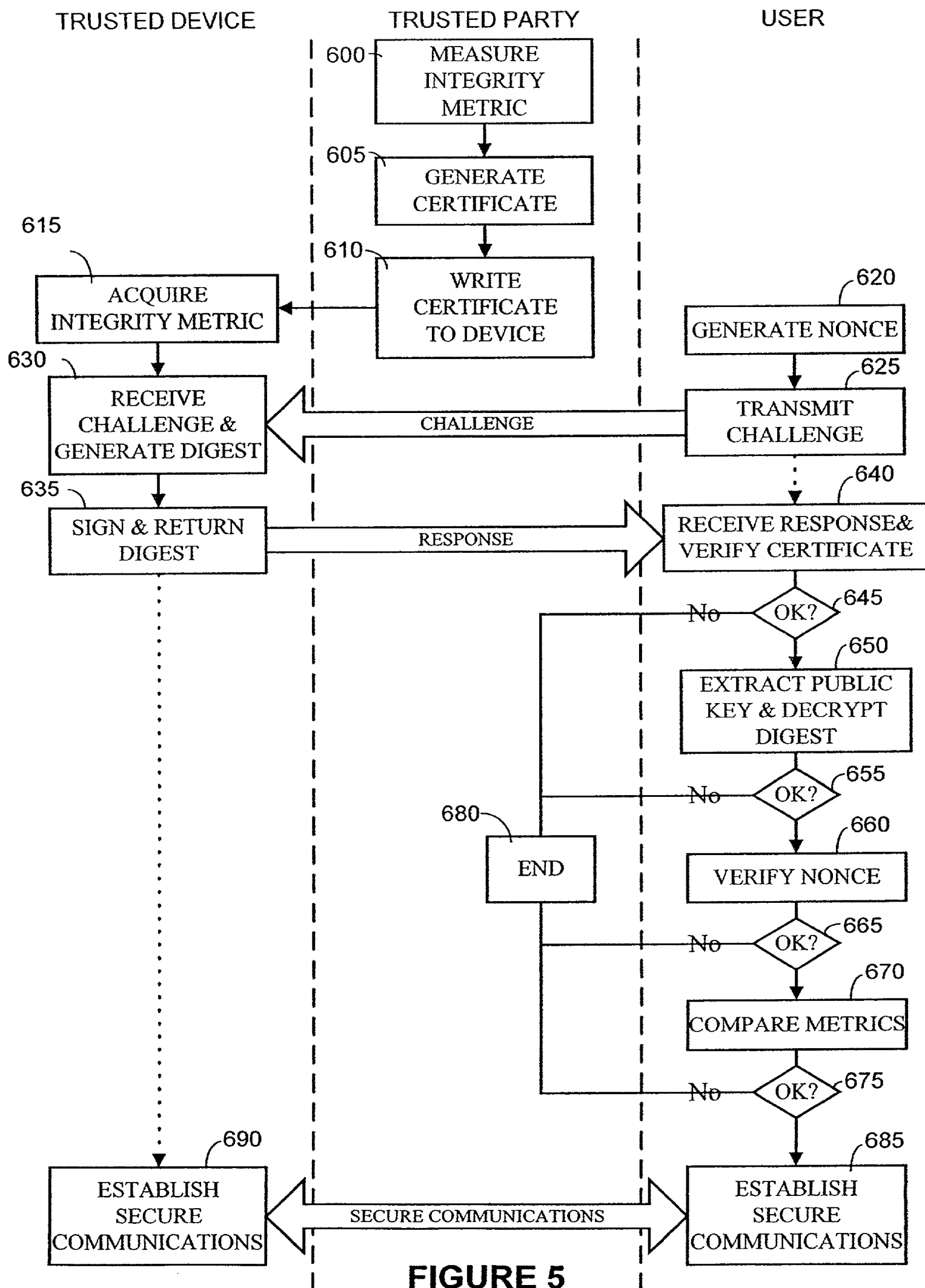


**FIGURE 3**

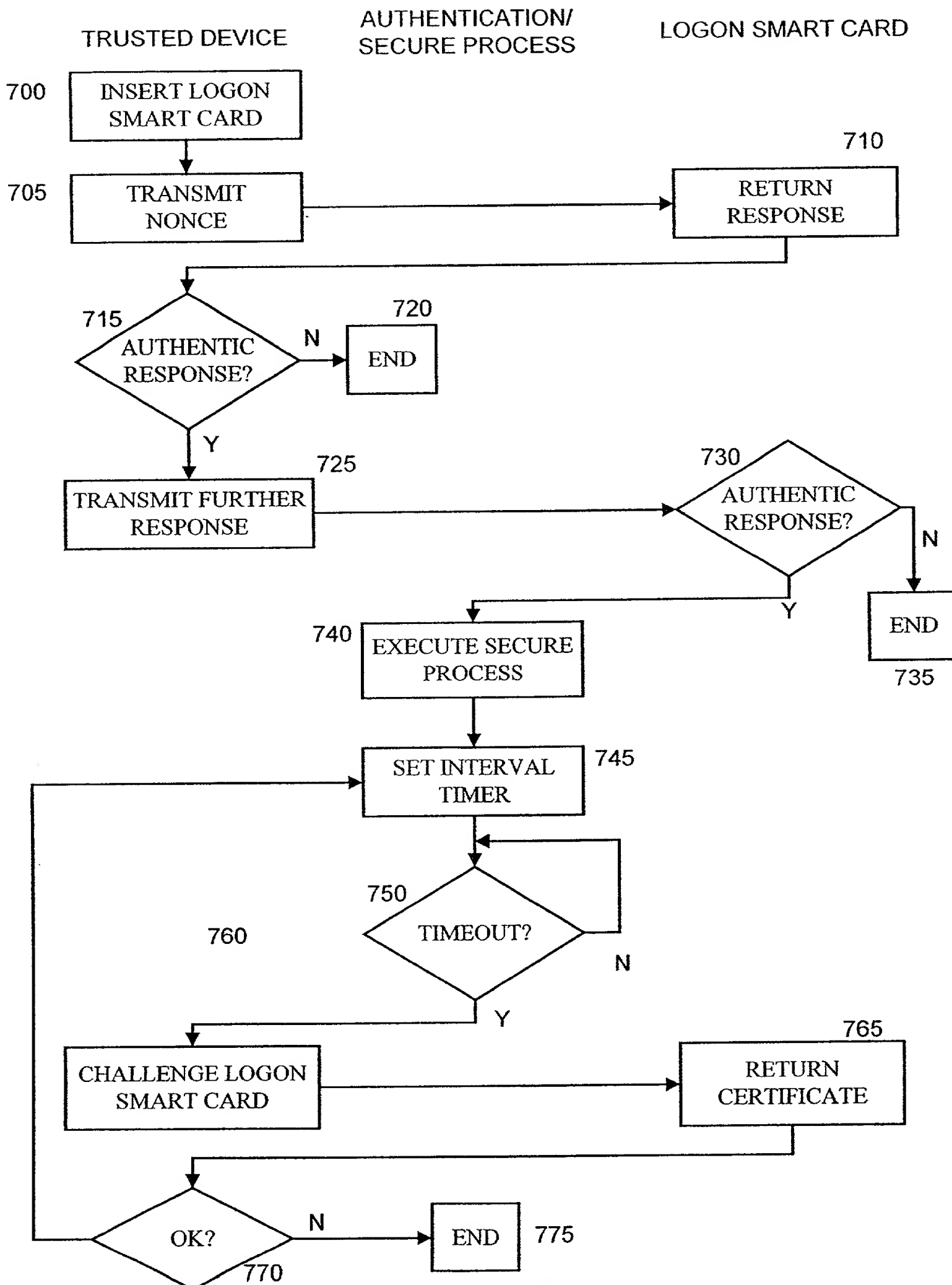
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**FIGURE 4**

4/5

**FIGURE 5**

5/5

**FIGURE 6**

**COMBINED DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY** ATTORNEY'S DOCKET No 30990050 US  
(Includes Reference to PCT International Applications)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Trusted Computing Platform

the specification of which was filed as PCT international application

PCT/GB00/00528

on 15 February 2000

and was amended under PCT Article 19

on ( if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, ' 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, ' 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

**PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:**

COUNTRY (if PCT indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
EP	99301100.6	15 February 1999	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
GB	9905056.9	5 March 1999	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, ' 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, ' 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, ' 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

**COMBINED DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY (Continued)**  
(Includes Reference to PCT International Applications)

**PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:**

U.S. APPLICATIONS		STATUS (Check one)		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.		
PCT APPLICATION NO.	PCT FILING DATE	U.S. SERIAL NUMBERS
ASSIGNED (if any)		

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Richard P. Berg, Reg.No. 28,

SEND CORRESPONDENCE TO:

IP Administration  
C/o Hewlett-Packard Company  
3404 East Harmony Road  
Mail Stop 35  
Ft. Collins, CO 80528-9599  
USA

DIRECT TELEPHONE CALLS TO:

Richard P. Berg (323) 934-2300

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: PROUDLER, Graeme John  
Inventor's Signature: *G. Proudler*

Dated: 20<sup>th</sup> August 2001

Residence: Bristol, United Kingdom  
Citizenship: GB  
Post Office Address: 5 Touchstone Avenue, Stoke Gifford, Bristol BS34 8XQ United Kingdom

Full name of 2nd joint inventor, if any: GUPTA, Dipankar  
Inventor's Signature:

Dated:

Residence: Mountain View, California, USA  
Citizenship: IN  
Post Office Address: 983 Sladky Ave, Mountain View, California 94040, USA

Full name of 3rd joint inventor, if any: CHEN, Liqun  
Inventor's Signature:

Dated:

Residence: Bristol, United Kingdom  
Citizenship: GB  
Post Office Address: 1 Harvest Close, Bradley Stoke, Bristol BS32 9DQ United Kingdom

Full name of 4th joint inventor, if any: PEARSON, Siani Lynne

Inventor's Signature: *Siani Pearson*

Dated: 13/08/01

Residence: Bristol, United Kingdom  
Citizenship: GB  
Post Office Address: 35 Sandyleaze, Westbury on Trym, Bristol, BS9 3PZ United Kingdom

Full name of 5th joint inventor, if any: BALACHEFF, Boris

Inventor's Signature:

Dated:

Residence: Bristol, United Kingdom  
Citizenship: FR  
Post Office Address: 7 Heathfield Close, Keynsham, Bristol BS31 2HJ United Kingdom

Full name of 6th joint inventor, if any: VAN WILDER, Bruno Edgard

Inventor's Signature:

Dated:

Residence: Aalst, Belgium  
Citizenship: BE  
Post Office Address: 1/3 Bauwensplaats, Aalst 9300, Belgium

Full name of 7th joint inventor, if any: CHAN, David

Inventor's Signature:

Dated:

Residence: Monte Sereno, California USA  
Citizenship: GB  
Post Office Address: 16112 Mays Avenue, Monte Sereno, California 95030, USA

3W Full name of 3rd joint inventor, if any: CHEN, Lijun

Inventor's Signature: 

Dated: 8/8/2001

Residence: Bristol, United Kingdom

Citizenship: GB

Post Office Address: 1 Harvest Close, Bradley Stoke, Bristol BS32 9DQ United Kingdom

Full name of 4th joint inventor, if any: PEARSON, Siani Lynne

Inventor's Signature:

Dated:

Residence: Bristol, United Kingdom

Citizenship: GB

Post Office Address: 35 Sandyleaze, Westbury on Trym, Bristol, BS9 3PZ United Kingdom

Full name of 5th joint inventor, if any: BALACHEFF, Boris

Inventor's Signature:

Dated:

Residence: Bristol, United Kingdom

Citizenship: FR

Post Office Address: 7 Heathfield Close, Keynsham, Bristol BS31 2HJ United Kingdom

Full name of 6th joint inventor, if any: VAN WILDER, Bruno Edgard

Inventor's Signature:

Dated:

Residence: Aalst, Belium

Citizenship: BE

Post Office Address: 1/3 Bauwensplaats, Aalst 9300, Belgium

Full name of 7th joint inventor, if any: CHAN, David

Inventor's Signature:

Dated:

Residence: Monte Sereno, California USA

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**COMBINED DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY (Continued)**  
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**PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:**

U.S. APPLICATIONS		STATUS (Check one)		
U S APPLICATION NUMBER	U S FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.		
PCT APPLICATION NO	PCT FILING DATE	U S SERIAL NUMBERS ASSIGNED (if any)

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Dated:

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Citizenship: GB

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Full name of 2nd joint inventor, if any: GUPTA, Dipankar

Inventor's Signature:

Dated: 27 Sep 2001

Residence: Fort Collins, Colorado, US

Citizenship: IN

Post Office Address: 525 Charrington Court, Fort Collins, CO 80525, USA

Full name of 3rd joint inventor, if any: CHEN, Lique

Inventor's Signature:

Dated:

Residence: Bristol, United Kingdom

Citizenship: GB

Post Office Address: 1 Harvest Close, Bradley Stoke, Bristol BS32 9DQ United Kingdom

Full name of 4th joint inventor, if any: PEARSON, Siani Lynne

Inventor's Signature:

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Post Office Address: 1/3 Bauwensplaats, Aalst 9300, Belgium

Full name of 7th joint inventor, if any: CHAN, David

Inventor's Signature:

Dated:

Residence: Monte Sereno, California USA

Citizenship: GB

Post Office Address: 16112 Mays Avenue, Monte Sereno, California 95030, USA

**COMBINED DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY** ATTORNEY'S DOCKET No 30990050 US  
(Includes Reference to PCT International Applications)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Trusted Computing Platform

the specification of which was filed as PCT international application

PCT/GB00/00528

on 15 February 2000

and was amended under PCT Article 19

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COUNTRY (if PCT indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
EP	99301100.6	15 February 1999	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
GB	9905056.9	5 March 1999	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, ' 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, ' 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, ' 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

**COMBINED DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY (Continued)**  
(Includes Reference to PCT International Applications)

**PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:**

U.S. APPLICATIONS		STATUS (Check one)		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.		
PCT APPLICATION NO.	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED (if any)

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Richard P. Berg, Reg.No. 28,

SEND CORRESPONDENCE TO:

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Mail Stop 35  
Ft. Collins, CO 80528-9599  
USA

DIRECT TELEPHONE CALLS TO:

Richard P. Berg (323) 934-2300

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Full name of sole or first inventor: PROUDLER, Graeme John

Inventor's Signature:

Dated:

Residence: Bristol, United Kingdom

Citizenship: GB

Post Office Address: 5 Touchstone Avenue, Stoke Gifford, Bristol BS34 8XQ United Kingdom

Full name of 2nd joint inventor, if any: GUPTA, Dipankar

Inventor's Signature:

Dated:

Residence: Mountain View, California, USA

Citizenship: IN

Post Office Address: 983 Sladky Ave, Mountain View, California 94040, USA

Full name of 3rd joint inventor, if any: CHEN, Liqun  
Inventor's Signature:

Dated:

Residence: Bristol, United Kingdom  
Citizenship: GB  
Post Office Address: 1 Harvest Close, Bradley Stoke, Bristol BS32 9DQ United Kingdom

Full name of 4th joint inventor, if any: PEARSON, Siani Lynne  
Inventor's Signature:

Dated:

Residence: Bristol, United Kingdom  
Citizenship: GB  
Post Office Address: 35 Sandyleaze, Westbury on Trym, Bristol, BS9 3PZ United Kingdom

Full name of 5th joint inventor, if any: BALACHEFF, Boris  
Inventor's Signature:

Dated:

Residence: Bristol, United Kingdom  
Citizenship: FR  
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Full name of 6th joint inventor, if any: VAN WILDER, Bruno Edgard  
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Dated:

Residence: Aalst, Belium  
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Full name of 7th joint inventor, if any: CHAN, David  
Inventor's Signature:

Dated: 10 Aug 01

Residence: Monte Sereno, California USA  
Citizenship: GB  
Post Office Address: 16112 Mays Avenue, Monte Sereno, California 95030, USA

**COMBINED DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY** ATTORNEY'S DOCKET No. 30990050 US  
(Includes Reference to PCT International Applications)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Trusted Computing Platform

the specification of which was filed as PCT international application

PCT/GB00/00528

on 15 February 2000

and was amended under PCT Article 19

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**PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:**

COUNTRY (if PCT indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
EP	99301100.6	15 February 1999	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
GB	9905056.9	5 March 1999	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No

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**COMBINED DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY (Continued)**  
(Includes Reference to PCT International Applications)

**PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:**

U.S. APPLICATIONS		STATUS (Check one)		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.		
PCT APPLICATION NO	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED (if any)

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Richard P. Berg, Reg.No. 28,

SEND CORRESPONDENCE TO:  
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C/o Hewlett-Packard Company  
3404 East Harmony Road  
Mail Stop 35  
Ft. Collins, CO 80528-9599  
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DIRECT TELEPHONE CALLS TO:  
Richard P. Berg (323) 934-2300

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Inventor's Signature:

Dated:

Residence: Bristol, United Kingdom  
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Post Office Address: 5 Touchstone Avenue, Stoke Gifford, Bristol BS34 8XQ United Kingdom

Full name of 2nd joint inventor, if any: GUPTA, Dipankar  
Inventor's Signature:

Dated:

Residence: Mountain View, California, USA  
Citizenship: IN  
Post Office Address: 983 Sladky Ave, Mountain View, California 94040, USA

**COMBINED DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY** ATTORNEY'S DOCKET No 30990050 US { PR  
(Includes Reference to PCT International Applications)

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My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Trusted Computing Platform

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Dated:

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Inventor's Signature:

Dated:

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Full name of 4th joint inventor, if any: PEARSON, Siani Lynne  
Inventor's Signature:

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Full name of 5th joint inventor, if any: BALACHEFF, Boris  
Inventor's Signature:

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5-10-01

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Inventor's Signature:

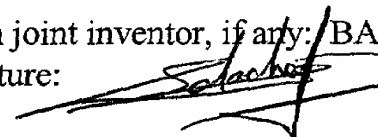
Dated:

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**COMBINED DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY** ATTORNEY'S DOCKET No 30990050 US  
(Includes Reference to PCT International Applications)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Trusted Computing Platform

the specification of which was filed as PCT international application

PCT/GB00/00528

on 15 February 2000

and was amended under PCT Article 19

on ( if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, ' 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, ' 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

**PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:**

COUNTRY (if PCT indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
EP	99301100.6	15 February 1999	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
GB	9905056.9	5 March 1999	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, ' 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, ' 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, ' 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application: